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Dynamic Analysis of Charge Separation in Metal-Insulator-Semiconductor Devices Used for High-Power Applications

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Abstract

In this study, a low-potential analysis of the charge separation dynamics in the metal-insulator-semiconductor (MIS) devices used for the architecture of the power electronic circuits, systems and networks. The separation events were supposed and analyzed at the interface regions within the bulk structures of such devices. The results of the performed analysis have shown that the charge separation may have reasonable effect on the performance and efficiency of the MIS device when the operation potentials are lower than 1 kV/m. Such potential values are the basement of the MIS power electronics employed in hyperfine electronics.

Keywords: Dynamic analysis; MIS devices; Power electronics; Charge separation

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1. Introduction

Power electronics still have their featured position in practical and industrial applications of electronics and their devices. Their efficient performance was obviously confirmed throughout their ability to produce stable and useful output [1,2]. However, the phenomena included in their performance, especially those related to the charge motion, distribution, interaction and compensation, were not intensively investigated [3,4]. Due to the inevitable existence of several surface and bulk regions within the electronic device, such phenomena should be thoroughly investigated and analyzed in order better performances and hence higher efficiencies can be achieved [5-7]. Otherwise, lower performances and efficiencies may still practical since the production economy and complexity cannot be compensated [8].

Among the most effective power electronic architectures, metal-insulator-semiconductor (MIS) devices are increasingly used and employed in modern bulk, fine and hyperfine technologies [9-13]. In case of bulk MIS devices and circuits, the phenomena of the charge motion, distribution, interaction and compensation may not be so much effective to change the performance parameters and affect the efficiencies [14,15]. Many research works and studies showed that such phenomena may cause lower than 0.05% variations in the values of overall efficiency at potential ranges higher than 10 kV/m. This value may increase to 0.1% at extraordinary potential ranges, those are not normally practical [16]. At potential ranges lower than 1 kV/m, variations of lower than 0.01% can be observed [17-20].

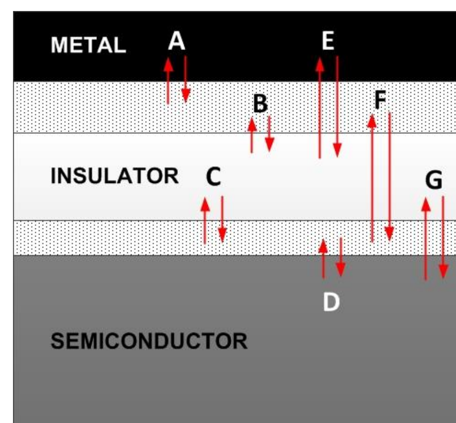

Fig. (1) Scheme of the MIS device analyzed in this study

Hyperfine technologies lead to make the variations in the performance and efficiencies relatively drastic and should be considered when the optimization of very-low-scale integration (VLSI)

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devices, circuits, systems and networks is required [21-22]. One of the most effective phenomena is the charge separation at the interfaces within the MIS structures [23,24]. Conceptually, there can be seven different modes of charge separation within such structures, as shown in Fig. (1). Such modes can occur totally or partially at the four interface regions shown (A, B, C and D). Additionally, charge dynamic and separation events can occur thoroughly from one terminal of the structure to another without functional events in the interface region (E, F, and G). These events certainly have different rates and probabilities as they are initiated under different potential schemes and hence move between different layers [25].

In this study, a low-potential analysis of the charge separation dynamics is presented for the optimization of MIS devices used for the architecture of power electronic circuits, systems and networks.

2. Experiment

A set of MIS devices were prepared by the programmable thermal evaporation method as multilayer structures. Figure (2) shows the SEM image of the fabricated device structure. The fabricated device with the structure of Al/M/AlO_x/Pt can be presented and materials of top electrode (TE) are Ni and TiN, respectively. Take the Al/TiN/AlO_x/Pt device as an example. At first, to remove the organic and inorganic impurities, the purchased substrate comprising Pt/Ti/SiO_2/Si was ultrasonically cleaned in acetone, ethanol, and DI water in sequence. The time for each ultrasonic cleaning process was 20 min. Then the 15-minute hydrophilic treatment in a vacuum with an expanded plasma cleaner (PDC-002 HARRICK PLASMA) was conducted to the cleaned Pt substrate, which enhanced the hydrophilia of the bottom electrode (BE) and made the entire spin-coating process easier to obtain.

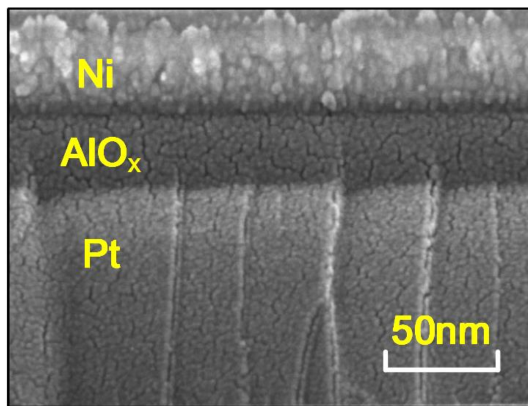

Fig. (2) SEM image of the MIS device fabricated in this study

After the process of hydrophilic treatment, the prepared 2.5 M AlO_x precursor solution was spin-coated in the air onto the Pt substrate with a spin rate at 3500 rpm and the spin time was 40 s. Then the device with the structure of AlO_x precursor solution/Pt was annealed at the desired temperature (225/250/275°C) for 60 min in the air and a ~ 35 nm AlO_x switching layer was grown successfully. Finally, a ~ 40 nm TiN layer and a ~ 20 nm Al layer were deposited onto the AlO_x layer by thermal evaporator respectively. The TiN was chosen as the TE layer while the capper layer Al was used to prevent the external oxidation. The TE layer was deposited onto the switching layer through a shadow mask and a single TE was deposited with the size of 0.1 mm diameter determined by the mask aperture.

3. Results and Discussion

The analysis of charge separation dynamics in this study may start from the rate equations at each interface region as follows [26]:

$$R_A = \left\{\mu_{eA}\frac{\partial\rho_e}{\partial t} + \mu_{hA}\frac{\partial\rho_h}{\partial t}\right\} \quad (1a)$$

$$R_B = \left\{\mu_{eB}\frac{\partial\rho_e}{\partial t} + \mu_{hB}\frac{\partial\rho_h}{\partial t}\right\} \quad (1b)$$

$$R_C = \left\{\mu_{eC}\frac{\partial\rho_e}{\partial t} + \mu_{hC}\frac{\partial\rho_h}{\partial t}\right\} \quad (1c)$$

$$R_D = \left\{\mu_{eD}\frac{\partial\rho_e}{\partial t} + \mu_{hD}\frac{\partial\rho_h}{\partial t}\right\} \quad (1d)$$

At the A interface [27]

$$\lim_{\rho_h\to 0}\left(\frac{\partial\rho_h}{\partial t}\right) \approx 0 \quad (3)$$

Therefore

$$R_A = \mu_{eA}\frac{\partial\rho_e}{\partial t} \quad (4)$$

At the B and C interfaces [28]

$$\rho_h < \rho_h \approx 0 \quad (5)$$

So,

$$R_B \approx 0 \quad (6a)$$

$$R_C \approx 0 \quad (6b)$$

For the E event

$$R_E = \left\{\mu_{eE}\frac{\partial\rho_e}{\partial t} + \mu_{hE}\frac{\partial\rho_h}{\partial t} - \Gamma_E\mu_{ehE}\frac{\partial\rho_{eh}}{\partial t}\right\} \quad (7)$$

For the F event

$$R_F = \left\{\mu_{eF}\frac{\partial\rho_e}{\partial t} + \mu_{hF}\frac{\partial\rho_h}{\partial t} - \Gamma_F\mu_{ehF}\frac{\partial\rho_{eh}}{\partial t}\right\} \quad (8)$$

For the G event

$$R_G = \left\{\mu_{eG}\frac{\partial\rho_e}{\partial t} + \mu_{hG}\frac{\partial\rho_h}{\partial t} - \Gamma_G\mu_{ehG}\frac{\partial\rho_{eh}}{\partial t}\right\} \quad (9)$$

Where Γ is the recombination (or decay) function, which describes the loss of charges during the dynamic event through the transient interfaces. This function can be determined experimentally at acceptable accuracy

For charges moving from the metal to the insulator through the M-I interface [29]

$$\lim_{\rho_h\to 0}\left(\frac{\partial\rho_h}{\partial t}\right) \approx 0 \quad (10)$$

Therefore

$$R_E = \left\{\mu_{eE}\frac{\partial\rho_e}{\partial t} - \Gamma_E\mu_{ehE}\frac{\partial\rho_{eh}}{\partial t}\right\} \quad (11)$$

Also

$$\mu_{eE}\frac{\partial\rho_e}{\partial t} \gg \Gamma_E\mu_{ehE}\frac{\partial\rho_{eh}}{\partial t} \quad (12)$$

Hence

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$$R_E \approx \mu_{eE} \frac{\partial \rho_e}{\partial t} \quad (13)$$

Similarly

For charges moving from the insulator to the semiconductor through the I-S interface

$$\lim_{\rho_e \to 0} \left(\frac{\partial \rho_e}{\partial t} \right) \approx 0 \quad (14)$$

Therefore

$$R_G = \left\{ \mu_{hG} \frac{\partial \rho_h}{\partial t} - \Gamma_G \mu_{ehG} \frac{\partial \rho e_h}{\partial t} \right\} \quad (15)$$

Also

$$\mu_{hG} \frac{\partial \rho_h}{\partial t} \gg \Gamma_G \mu_{ehG} \frac{\partial \rho_{eh}}{\partial t} \quad (16)$$

Hence

$$R_G = \mu_{hG} \frac{\partial \rho_h}{\partial t} \quad (17)$$

For charges moving through the insulator layer from metal to the semiconductor and vice versa [30]

$$\mu_{eF} \frac{\partial \rho_e}{\partial t} \approx \mu_{hF} \frac{\partial \rho_h}{\partial t} \quad (18a)$$

$$\Gamma_F \mu_{ehF} \frac{\partial \rho_{eh}}{\partial t} \approx 0 \quad (18b)$$

Therefore

$$R_F = 2\mu_{eF} \frac{\partial \rho_e}{\partial t} \quad (19)$$

Combining all rates, we can obtain

$$R = R_A + R_D + R_E + R_F + R_G \quad (20)$$

$$R = \mu_{eA} \frac{\partial \rho_e}{\partial t} + \mu_{eD} \frac{\partial \rho_e}{\partial t} + \mu_{hD} \frac{\partial \rho_h}{\partial t} + \mu_{eE} \frac{\partial \rho_e}{\partial t} + 2\mu_{eF} \frac{\partial \rho_e}{\partial t} + \mu_{hG} \frac{\partial \rho_h}{\partial t}$$

$$R = 5\mu_e \frac{\partial \rho_e}{\partial t} + 2\mu_h \frac{\partial \rho_h}{\partial t} \quad (21)$$

Figures (3) show the total rate of charge separation as a function of charge mobility for both types of charges existing in the MIS structure. The systematic behavior of the separation rate is not the actual situation because the charge dynamics in the MIS (and mostly all hybrid structures) are correlated due to static and dynamics electrical forces in addition to the effect of varying densities throughout the fabricated structure [31].

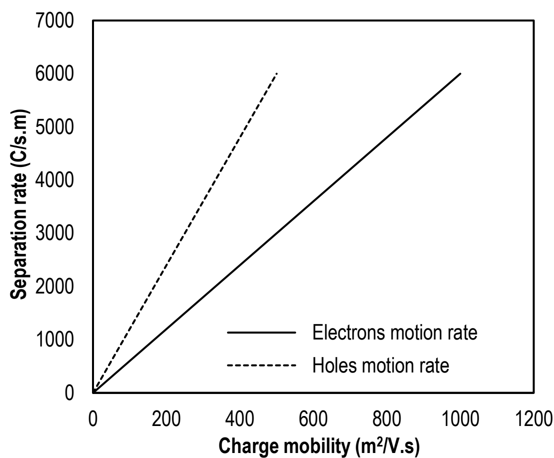

Fig. (3) Variation of separation rate with the charge mobility without correlation between charge dynamics

Taking the correlation between charge dynamics into account, the variation of charge separation rate with charge mobilities can be shown in Fig. (4). A kind of irregularity can be observed at the initial values of charge motion throughout the MIS structure when the potential is critically sufficient to overcome the static and dynamic forces mentioned before.

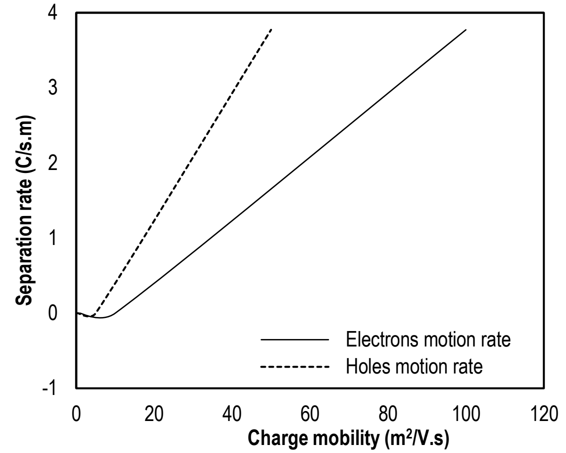

Fig. (3) Variation of separation rate with the charge mobility with correlation between charge dynamics

4. Conclusion

In concluding remarks, a low-potential analysis of the charge separation dynamics in the metal-insulator-semiconductor (MIS) devices used for the architecture of the power electronic circuits, systems and networks. The separation events were supposed and analyzed at the interface regions within the bulk structures of such devices. The results of the performed analysis have shown that the charge separation may have reasonable effect on the performance and efficiency of the MIS device when the operation potentials are lower than 1 kV/m. Such potential values are the basement of the MIS power electronics employed in hyperfine electronics.

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